REMARKS

Claims 36, 44, and 55 have been amended. Claims 29-32 and 34-35 have been canceled. Claims 66-73 are new. Claims 36-39, 41, 44-47, 49, 51-59 and 65-73 are currently pending in this application. Applicant thanks the Examiner for the allowance of claims 59 and 65. Applicant reserves the right to pursue the original and other claims in this and other applications. Applicant respectfully requests reconsideration in light of the above amendments and the following remarks.

The claimed invention relates to an electropolished patterned metal layer formed as a lower electrode of a capacitor, which may be part of a semiconductor device, such as a memory cell, or a processor-based system. The electropolished metal layer of the claimed invention allows for high resolution patterning with increased processing accuracy in the patterning of noble metals. Specification, page 8, lines 5-10. As shown in FIG. 14 (reproduced below), the electropolished lower electrode 70 is formed such that it is fully within a contact opening (41, FIG. 7) within insulating layer 25. The capacitor 100 also includes a barrier conductive layer 60 between the insulating layer 25 and the lower electrode 70. A dielectric layer 72 is formed over the lower electrode 70. Upper electrode 74 is formed over dielectric layer 72. Protective barrier layer 52 may also be provided beneath the capacitor 100.

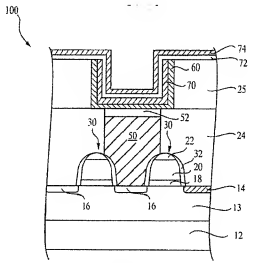

FIG. 14

Claims 55 and 56 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Fazan et al. (U.S. Patent No. 5,976,928) ("Fazan"). This rejection is respectfully traversed.

Claim 55 recites a container capacitor including a "first metal barrier layer provided fully within a first insulating layer, said barrier layer having a bottom wall and vertical sidewalls extending rectangularly upwardly therefrom," a "lower electrode provided fully within said first insulating layer and over said first metal barrier layer, said lower electrode comprising an electropolished patterned metal layer having a bottom wall and vertical sidewalls extending rectangularly upwardly therefrom," a "second insulating layer provided over said electropolished patterned metal layer and in contact with said first insulating layer" and an "upper electrode provided over said second insulating layer."

Applicant respectfully submits that Fazan does not disclose the "first metal barrier layer provided fully within a first insulating layer, said barrier layer having a bottom wall and vertical sidewalls extending rectangularly upwardly therefrom." The capacitor of Fazan includes a second insulation layer 83 with an opening wherein a platinum layer 85, dielectric layer 87 and cell plate layer 88 are located. *See*, Fazan, col. 7, lines 50-65 and FIG. 14B. However, Fazan does not disclose a "first metal barrier layer provided fully within a first insulating layer, said barrier layer having a bottom wall and vertical sidewalls extending rectangularly upwardly therefrom," as recited by claim 55. Accordingly, claim 55 is allowable over Fazan. Claim 56 depends from claim 55 and is allowable along with claim 55. Applicant respectfully requests that the rejection of claims 55 and 56 be withdrawn and the claims allowed.

Claims 29-32, 34 and 35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Jeng et al. (U.S. Patent No. 6,184,081) in view of Fazan. Claims 29-32, 34 and 35 have been canceled; thus this rejection is moot.

Claims 36-39, 41, 44-47, 49 and 51-52 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fazan in view of Taniguchi (U.S. Patent No. 6,559,494) ("Taniguchi"). This rejection is respectfully traversed.

Claim 36 recites a memory cell comprising a "transistor including a gate fabricated on a semiconductor substrate and including a source/drain region in said semiconductor substrate disposed adjacent to said gate," an "insulating layer provided over said substrate" and a "container capacitor." The capacitor includes a "first metal barrier layer, a lower electrode over said first metal barrier layer, a dielectric layer over said lower electrode, and an upper electrode over said dielectric layer, said upper electrode comprising doped polysilicon, and said lower electrode having a surface aligned over said source/drain region." The "said first metal barrier layer is fully within said insulating layer," and the "lower electrode comprises an electropolished patterned metal layer which is situated fully within said insulating layer, [and] … has a thickness of about 50 to about 300 Angstroms." Further, the "dielectric layer is in contact with said insulating layer."

Claim 44 recites a processor-based system including a "processor" and an "integrated circuit coupled to said processor." Further, "at least one of said integrated circuit and said processor compris[e] a container capacitor provided within an insulating layer, said container capacitor including a first metal barrier layer, a lower electrode and an upper electrode, said lower electrode comprising an electropolished patterned metal layer having a thickness of approximately 50 to 300 Angstroms, wherein a top surface of said electropolished patterned metal layer and said first metal barrier layer are at the same level with a top surface of said insulating layer such that said lower electrode and said first metal barrier layer do not extend above the top surface of said insulating layer."

The capacitor of Fazan includes second insulation layer 83 with an opening wherein a platinum layer 85, dielectric layer 87 and cell plate layer 88 are located. *See*, Fazan, col. 7, lines 50-65 and FIG. 14B. However, Fazan does not disclose a "first metal barrier layer, a lower electrode over said first metal barrier layer, a dielectric layer over said lower electrode, and an upper electrode over said dielectric layer …[where] said first metal barrier layer is fully within said insulating layer," as recited by claim 36. Nor does Fazan disclose "a first metal barrier layer, [and] a lower electrode [where] said first metal barrier layer [is] at the same level with a top surface of said insulating layer such that said lower electrode and said first metal barrier layer do not extend above the top surface of said insulating layer," as recited by claim 44.

Taniguchi, which has been cited as teaching an upper electrode comprising doped polysilicon, does not cure the deficiencies of Fazan discussed above. Since the Fazan and Taniguchi combination does not teach or suggest all of the limitations of claims 36 and 44, claims 36 and 44 are not obvious over the cited references. Claims 37-39 and 41 depend from claim 36 and are allowable along with claim 36. Claims 45-47, 49 and 51-52 depend from claim 44 and are allowable along with claim 44. Applicant respectfully requests that the rejection of claims 36-39, 41, 44-47, 49 and 51-52 be withdrawn and the claims allowed.

Claims 53 and 54 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fazan in view of Taniguchi and Hashimoto (U.S. Patent No. 6,515,370) ("Hashimoto"). This rejection is respectfully traversed. Claims 53 and 54 depend from claim 44 and are patentable over Fazan and Taniguchi for at least the reasons mentioned above. Hashimoto, which has been cited as teaching the fabrication of specific memory devices, does not cure the deficiencies of Fazan discussed above. Applicant respectfully requests that the rejection of claims 53 and 54 be withdrawn and the claims allowed.

Claims 57 and 58 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fazan. This rejection is respectfully traversed. Claims 57 and 58 depend from claim 55, which is are patentable over Fazan for at least the reasons mentioned above. Applicant respectfully requests that the rejection of claims 57 and 58 be withdrawn and the claims allowed.

In view of the above, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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